

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): PARENT et al.

Serial No.: 10/799,742

Group Art Unit: 2827

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Filed: March 12, 2004

DEC 23 2005

Title: Method and Circuit for Reducing
Defect Current From Array Element
Failures in Random Access Memories

Examiner: Mai, Son Luu

Attorney Docket No.: CD03011

RESPONSE TO FINAL OFFICE ACTION

5 Mail Stop AF
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

10 A. Introductory Comments

The following is submitted in response to the FINAL Office Action dated October 31, 2005. The two month Advisory Action period ends January 3, 2006.

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37 C.F.R. §1.8

I hereby certify that this correspondence is being

30 transmitted via facsimile to the United States Patent and Trademark Office to fax number: 1-571-273-8300
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35 deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents,
 P.O. Box 1450, Alexandria VA 22313-1450.

Date of Deposit: _____

Typed/Printed Name: Bradley T. Sako40 Signature: 

The entry is denied by Examiner